BETA GALLIUM OXIDE MATERIALS PROCESSING AND DEVICE APPLICATIONS

A Thesis

Presented to the Faculty of the Graduate School

of Cornell University

In Partial Fulfillment of the Requirements for the Degree of

Master of Science

by

Liheng Zhang

August 2017

ABSTRACT

β-Ga_2O_3 recently gained much attention for its promising future for high-power electronic devices due to its ultra-wide bandgap (~4.9 eV), high breakdown field (~8MV/cm) and commercially available high-quality single-crystal wafers. Its Baliga's Figure of Merit (BFOM) is ~4 times as large as those of GaN and SiC for power efficiency. However, material processing is still in its infancy for high-performance devices fabrication. In this work, I explore different regions of processing conditions. Particularly, dry etching and Ohmic contact are studied and optimized for device fabrication. Electronic devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs) and vertical wrap-around-gate fin-shape FETs (vFinFETs) are fabricated using optimized processing conditions and achieved current modulations.

BIOGRAPHICAL SKETCH

Mr. Liheng Zhang was born in China and attended school there until he finished high school. Then he came to the United States to attend college. He studied Materials Science and Engineering at University of California Loa Angles (UCLA) for his undergraduate degree and graduated with the third highest honor (Cum Laude). He was under the advise of Professor Dwight Streit at UCLA and did some research on the material synthesis and optoelectronic properties of earth-abundant nitrides.

After finishing his Bachelor's degree, Liheng came to Cornell University in New York State to continue studying Material Science and Engineering for a Master of Science degree. He worked under Professor Debdeep Jena and Professor Grace Xing on wide-bandgap semiconductor materials and device applications. During his time at Cornell, he published a journal paper on the Japanese Journal of Applied Physics (JJAP) on his study on the dry etching behavior of gallium oxide.

Liheng will finish his Master thesis by June 2017.

To,

My family, and

friends.

ACKNOWLEDGMENTS

There are too many individuals that I need to thank for the completion of my master's thesis.

First, I want to thank DJ and Grace for giving me the opportunity to work in their excellent group and to work on my favorite topic, semiconductors. During the path of last two year, they have given me valuable advices on the direction of my research and generous support on the experiments I needed to conduct to finish my thesis. I could not have been such a knowledgeable and passionate scholar on semiconductors without their support and enlightenment.

Second, I want to thank all the senior group members in the Jena-Xing Group that haven given me countless helps for my project. Kazuki, Rusen, Mingda Zhu, Zongyang, and Wenshen gave me indispensible help on devices and processing. Vlad trained me on all the instruments. Kevin and Nick on the MBE growths needed for my sample. Also, everybody on being not only great lab mates but also close friends during my time at Cornell especially. Thank Sam for inviting me multiple times to his house to enjoy free and delicious home-made food.

Third, I want to thank all the staff members at Cornell NanoScale Science Technology Facility (CNF) that have helped me on all the tools I needed for my research. Working at CNF has been a major part of my project and without their experiences on cleanroom operations, I could not have made my work at CNF so smooth. My work made use of the Cornell NanoScale Science and Technology Facility (CNF) which is supported through the NSF NNCI program (Grant Number ECCS-1542081).

Fourth, I gratefully thank my parents for their continuing support for my pursuit of my academic goals and their insightful advices on my growing-up as a strong, kind and responsible adult. Without their support and wisdom, none of what I have achieved could have been possible.

Last but not least, I thank the NSF DMREF program (Award Number 1534303) for funding my research.

TABLE OF CONTENTS

Chapter 1: Introduction 1
1.1 β-Ga_2O_3 2
1.2 This work. 2
1.3 Related research 4
Chapter 2: Ohmic contacts 7
2.1 Si-ion-implantation 8
2.2 MBE regrown contact 13
Chapter 3: Dry etching 20
Chapter 4: Device applications 30
4.1 MOSFETs 30
4.2 Vertical FinFETs 37
Chapter 5: Conclusion 38
References **40**

CHAPTER 1

Introduction

Semiconductors have changed the way human beings live. They have brought people closer by providing ultra-speed communications and have created the Information Age by enabling fast computation and high-density information storage. They are the fundamental building blocks in every electronic system. The research of semiconductors started from elemental materials like germanium and silicon and then developed into the search for an entire zoo of compound semiconductors and their alloys. Compound semiconductors have many advantages over elemental ones because of their rich properties resulted from combining heterogeneous elements in the same lattice. The early generations of III-V materials such as GaAs and InP have brought the fastest devices for communication and are now commercialized. [1,2] The newer GaN based materials have shown great potential in optoelectronics for solid-state lighting as well as in electronics for high-power transmission. [3,4] The oxides are a new family of semiconductors that provide unique properties even beyond the III-Vs. Because of their large bandgaps, they usually possess larger breakdown fields than the III-Vs, which makes them very attractive for high-power applications.[10] Also, because of the large bandgaps, these oxides are transparent in the deep ultraviolet (UV) range, which makes a whole zoo of deep UV optoelectronic applications possible.[5] Ga_2O_3 is one member of these transparent conducting oxides (TCOs) that recently gained much attention for its unique properties as a semiconductor and its great potentials in high-power electronic and deep UV optoelectronic applications. [6,10] This work will focus on this material and its applications in high-power electronics.

1.1 β-Ga_2O_3[1]

(The content of this Section 1.1 is published in JJAP [23])

Wide bandgap semiconductors such as SiC and GaN are being pursued to replace Si in power electronic devices for the simultaneous miniaturization and improvements in the efficiency and system performance.[7-9] Recently, a new wide-bandgap semiconductor β-Ga_2O_3 has attracted much attention because of its potential to exceed both SiC and GaN in high-voltage devices.[10]β-Ga_2O_3 has a large bandgap E_g (~4.5-4.9 eV) and high estimated breakdown field F_{br} (~8 MV/cm).[10]Because of its superior material properties, its Baliga's figure of merit is four times or more as large as those for SiC or GaN, indicating that Ga_2O_3 has the potential to outperform SiC and GaN power devices.[10]Moreover, bulk crystals of Ga_2O_3 have been recently grown by traditional melt grown methods such as Chochralski,[11,12]edge-defined film fed (EFG) growth[13] and floating zone.[14,15] Consequently, high quality single crystal substrates of β-Ga_2O_3 of 4-in. diameter have become commercially available.[10]The availability of large area bulk crystals of β-Ga_2O_3 makes it economically competitive to other wide-bandgap semiconductor technologies currently being pursued for power electronics.

1.2 This work

Despite the great material properties, material processing for β-Ga_2O_3 is still in its infancy. Lateral FETs have been successfully fabricated but at early stages, their current levels were limited by large contact resistances at the source and drain.[16]

[1]

Therefore, developing low-contact resistance Ohmic is critical for boosting current density in high power devices. In this work, successful developments of such effective Ohmic contact using both regrowth and ion-implantation are presented in the first section of Chapter 2.

For high-power electronics, vertical devices are more attractive for its higher breakdown voltage and better scaling ability than lateral ones. However, only vertical Schottky barrier diodes (SBDs) on Ga_2O_3 have been studied but no vertical FETs have been reported to date. [17-19]However, vertical FETs on β-Ga_2O_3 is more challenging than on other material systems like GaN because p-type β-Ga_2O_3 has not been realized because of strong self-trapping of holes in this material but a p-type current-blocking layer is usually necessary in vertical FETs. [20,21] Therefore, realizing vertical FETs need to seek other paths like using ion-implantation as current blocking layer or creating a "fin" as the current channel to make vertical FinFETs with wrap-around gate.[22] The FinFET structure imposes challenges on etching conditions because the resulting fin needs to have vertical and smooth sidewalls.[22] In the second section of Chapter 2, I present systematic study on the dry etch behavior of Ga_2O_3.[23]

In Chapter 4, metal-oxide-semiconductor FETs (MOSFETs) are studied by fabricating devices with the optimized processes. The MOSFET's channel became insulating because of Fe out-diffusion from the semi-insulating substrate following dopant activation. An overlapping gate is fabricated to turn the device into E-mode with a ~10^6 on/off. Vertical FinFETs with wrap-around gate is also fabricated using the optimized dry etch process. Vertical fin-channels were successfully made and both ionic-gated and solid-state-gated devices had minor channel modulation (<10%) due to large channel width.

1.3 Related research

The research for Ga2O3 power devices started after 2010.[10] Sasaki et al first demonstrated a Schottky barrier diode (SBD) on single crystal with near-unity ideality factor and ~150V breakdown voltage.[17] With high-quality HVPE drifting layer and field-plate, Konishi et al achieved an SBD with >1kV breakdown voltage.[19] For three-terminal devices, Higashiwaki et al first demonstrated metal-semiconductor FETs (MESFETs) on molecular-beam-epitaxy (MBE) grown single crystal film with ~10000 on/off ratio and >250V breakdown voltage.[16] The on/off ratio was limited by relatively large contact resistance and lack of surface passivation.[16] The same group improved these drawbacks by making metal-oxide-semiconductor FETs (MOSFETs) on Si-ion-implanted channel with ion-implanted contact and achieved enhanced current level, 10^{10} on/off ratio and 415 V breakdown voltage.[10] These MOSFETs maintained normal device operation at an elevated temperature of 250 C° with 10^4 on/off ratio.[10] Later, they demonstrated field-plate (FP) MOSFETs with a record high >750V breakdown voltage.[24] Non-planar structures of the transistors were also attempted by Chabak el al who made enhancement-mode wrap-gate FinFETs with 10^5 on/off ratio and >600V breakdown voltage, highest for all non-planar FETs as they claimed.[25] The availability of nanomembrane by exfoliating in the (100) direction in Ga_2O_3 also enabled novel device fabrication.[26] Hwang et al demonstrated the first nanomembrane FET that can potentially be integrated on multiple platforms and that can switch relatively high voltage (>70V).[26] Zhou et al realized both Depletion- and Enhancement-mode nanomembrane FETs by controlling the thickness of membranes.[27,28] They achieved record high current densities of 1.5/1.0A/mm for D/E-

mode FETs due to high doping in the channel and improved Ohmic contacts by Ar bombardment.[28] Although Ga_2O_3 power devices have yet to exceeded GaN and SiC, the early stage of their development has already shown great promise for the future. For example, Green et al demonstrated a MOSFET with a 3.8 MV/cm breakdown field, highest among all transistors and already surpassing GaN's and SiC's theoretical limits.[29]

Key material processing techniques such as Ohmic contact, etching and gate dielectrics have been developed along the way the devices were demonstrated. Good Ohmic contacts have been realized by multiple methods. Higashiwaki et al found that reactive-ion etching (RIE) treatment before contact metal deposition can significantly reduce contact resistance (R_c) possibly due to large density of donor type defects created on the surface.[16] Zhou et al found that Ar bombardment on Ga_2O_3 surface could improve contact resistance in a similar way and that by using high-doping channel, R_c can be significantly reduced due to enhanced tunneling underneath the contact.[27,28]The R_c reported with $8*10^{18}$ cm^{-3} channel doping is 0.75 Ω-mm.[28] Oshima et al used an indium-tin oxide (ITO) layer on Ga_2O_3 to achieve Ohmic contact because of interdiffusion between the two materials following annealing.[30] Zeng et al used a similar method but using Sn-doped spin-on glass (SOG) as contact layer and achieved a specific contact resistivity of ~$2.1*10^{-5}$ Ω-cm^2.[31] Sasaki et al optimized dose and activation temperature for Si-ion-implantation contacts and achieved an R_c ~0.15 Ω-mm, lowest reported.[32] These contact technologies have been successfully used to fabricate transistors that demonstrated excellent device operations. [10, 27.28,31]

Both wet and dry etching have been studied to their impact on electrical properties of materials and device fabrication. Liang et al. studied the effect of SF_6/Ar gas ratio on Ga_2O_3 etch rate and surface morphology using inductively-coupled plasma (ICP).[33] They found that SF_6 is the main etching species with Ar assisting to remove non-volatile etch products and that by tuning the SF_6/Ar ratio, surface damage could be minimized.[33] Zhou et al. used RIE in NF_3 and Cl_2/Ar etchant gases and found that NF_3 gives higher etch rate.[34]Hogan et al. compared RIE with ICP on the etch behavior of different crystal planes of Ga_2O_3 and found that ICP gives better surface morphology and higher etch rate using Cl-based chemistry.[35] They also found that BCl_3 is the main etchant in the BCl_3/Cl_2 mixture and that the (010) and (-201) planes etch much faster than the (100) plane.[35] Yang et al found that surface damage increases proportionally with ICP etch rate.[36] Wet etchant including hydrofluoric acid (HF), hydrochloric acid (HCl) and phosphoric acid (H_3PO_4) have been shown to have negligible etch rate at room temperature due to the chemical inertness of Ga_2O_3.[37] These studies shed lights on the importance of etch conditions control on device performances.

CHAPTER 2

Ohmic Contacts

Ohmic contacts are a critical part in high-performance devices especially in power devices. Good Ohmic contacts eliminate significant voltage drop across the contact areas underneath source and drain in an FET so the entire applied voltage can be used to create currents in the channel. For similar material systems such as GaN, good Ohmic contacts have been achieved using several methods. Because of the large iconicity of GaN, it does not suffer Fermi-level pinning at the interface.[39] Therefore, the Schottky barrier height depends entirely on the work function difference between GaN and the metal. Therefore, good Ohmic contact can be achieved by choosing a metal with a work function smaller than that of GaN like Al and linear I-V behavior and a specific contact resistivity of 10^{-7}~10^{-8} Ω-m^2 have been achieved by depositing Al on GaN as contacts.[39] Even better Ohmic contacts can be achieved by molecular-beam-epitaxy (MBE) regrowing a highly doped n-type layer at the source and drain to facilitate tunneling.[40] This technique has been widely used in high-electron-mobility transistors (HEMTs) and the contact resistance can be as low as 0.16 Ω-mm.[40]

For Ga_2O_3, the first transistors were made using alloyed metal contact with pre-metal-deposition dry etching. [16] These contacts has linear I-V behavior but still limited the drain current because of relatively large contact resistance.[16] Sasaki et al. used Si-ion-implantation to achieve a specific contact resistivity of $4.6*10^{-6}$ Ω-cm^2 on the (010) face, lowest in literature for Ga_2O_3. [32] MOSFETs made using ion-implanted

contacts showed significantly enhanced drain current density. [10] However, Ohmic contact study on another commercially available crystal orientation, (-201), of Ga_2O_3 has not yet been reported so I studied contact resistance on the (-201) using Si-ion-implantation. This work will be presented in next section. Also, Ohmic contacts using ion-implantation can be vulnerable to damages caused by high ion energy and high activation temperature can also cause problems in device fabrications. Therefore, I used another method, the MBE regrown contacts, to study the contact resistance as well. This will be presented in the section following next section.

2.1 Si-ion implantation

Si ions are implanted in to 5mm x 5mm unintentionally-doped (UID) bulk Ga_2O_3 substrates for a depth of 150nm. Both (-201) and (010) substrates are used for comparison. Multiple ion doses, $5*10^{13}$ cm^{-2}, $1*10^{14}$ cm^{-2}, $2.3*10^{14}$ cm^{-2} and $6*10^{14}$ cm^{-2} are used with acceleration energies of 30kV, 50kV, 100kV and 180kV, respectively, to create a box profile of ion concentration of $5*10^{19}$ cm^{-3} in the first 150nm from the substrate surface. To put the peak concentration at the surface of Ga_2O_3, a 40nm SiO2 cap is deposited using plasma-enhanced chemical-vapor-deposition (PECVD). The simulated dopant profile versus depth is plotted in Figure 2.1. The dopants are activated by annealing in N_2 at 800 ~ 1000 C° (in steps of 50 C°) on five separate samples for (-201) face and 900 ~ 1100 C° (in steps of 100 C°) on (010) face on three separate samples for 30 minutes to obtain the optimized activation temperature.

Circular transmission line measurements (CTLM) are done by ebeam evaporating Ti/Au 50/100 nm metal stack to form inner and outer pads with a series of spacings (5, 7, 10, 12, 15, 20 μm). Figure 2.2 shows the optical image of the fabricated test structure and Figure 2.3 shows the cross-section of the ion-implanted substrate. The I-V measurements are done in four-point configuration to minimize the effect of contact resistance between probes and metal (also see Figure 2.2).

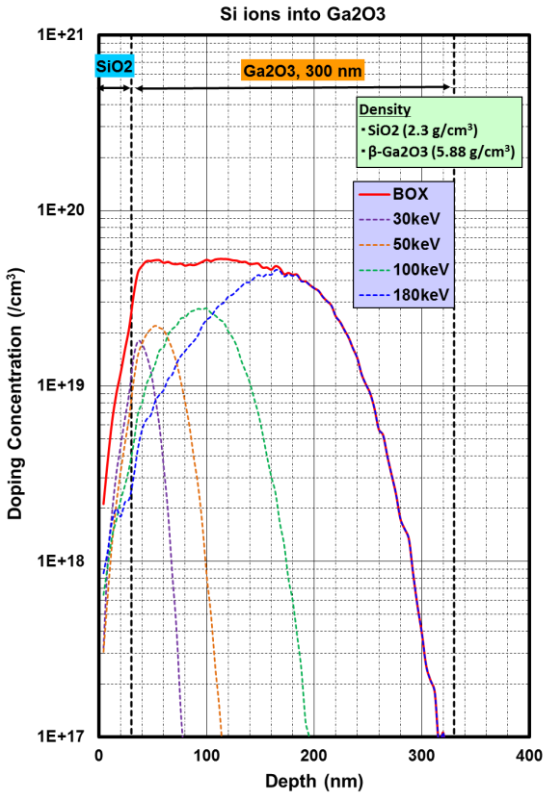

Figure 2.1 SRIM simulation of Si concentration profile.

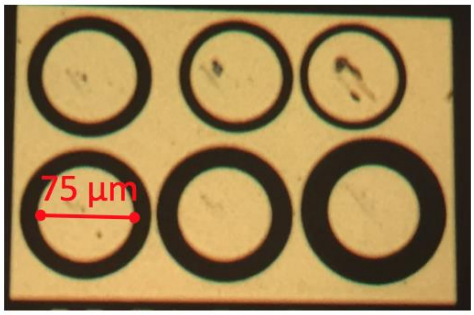

Figure 2.2 CTLM test structures.

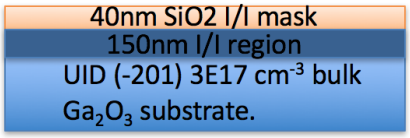

Figure 2.3 Cross-section of Si-ion-implanted samples.

Figure 2.4 plots the I-V at different spacings and the total-resistance vs spacing relationship for both (-201) and (010). For (-201), the best result is obtained at 900 C° while for (010), the best at 1000 C°. Only the plots at optimized temperature are presented here. At the optimized temperature, the I-Vs for both faces are perfectly linear and symmetrical, indicating a disappeared Schottky barrier at the metal/semiconductor interface. This is achieved because the layer in contact with metal becomes highly-doped with n-type carriers after the Si dopants are activated and therefore tunneling is promoted. From the R vs d plots, the total resistance is well scaled with spacing indicating high material quality and successful current confinement. The specific contact resistivity ρ_c and sheet resistance R_{sh} are extracted from the y-intercept and the slope of the R vs d plots, respectively, using the following equation:

$$\frac{R_{tot}}{C} = R_{sh} * \frac{(d + 2L_T)}{2 * \pi * L} \tag{2.1}$$

where R_{tot} is corrected for a geometric factor C for the circular shape, d is the spacing between inner and outer pads, L_T is the transfer length and L is the fixed radius or the inner pads. C is calculated using the relationship:

$$C = \left(\frac{L}{d}\right) * \ln\left(1 + \left(\frac{d}{l}\right)\right). \tag{2.2}$$

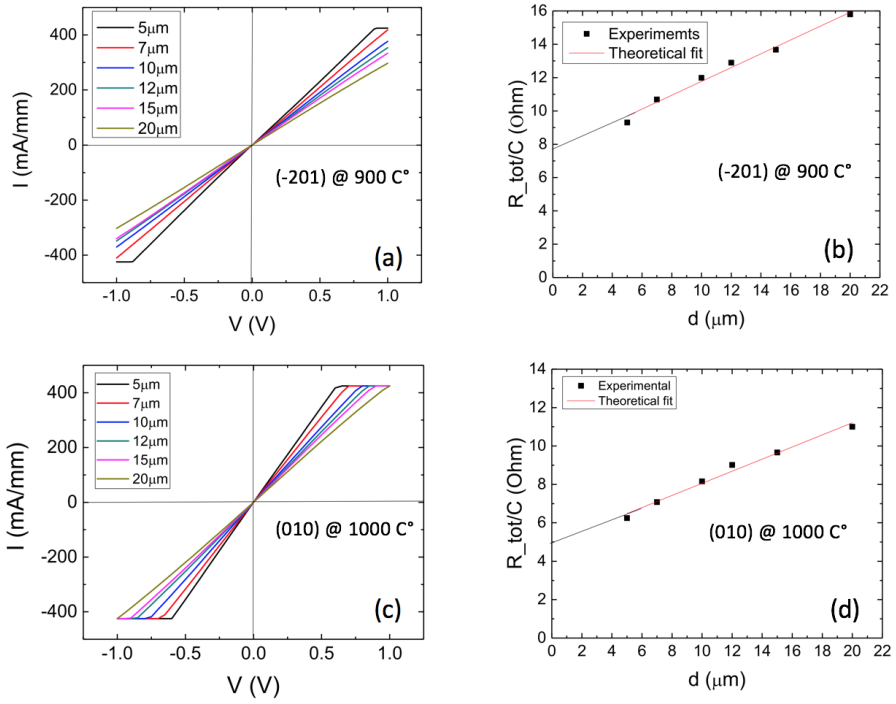

Figure 2.4 (a) I-V for (-201); (b) Geometry-corrected R_{tot} vs d for (-201); (c) I-V for (010); (d) Geometry-corrected R_{tot} vs d for (010).

For (010) face, specific contact resistance is $4.5*10^{-5}$ Ω-cm^2 and contact resistance is 0.58 Ω-mm at 1000 C°. These are the lowest among all activation temperatures and also at 1000 C°, the I-V characteristic is the most linear. In comparison to the results ($4.6*10^{-6}$ Ω-cm^2 and ~0.17 Ω-mm) obtained by Sasaki et al. who used the same Si dose and 950 C° activation temperature, our contact resistance is ~3 times higher and specific contact resistivity an order of magnitude higher.[32)] This could possibly due to

the fact that Sasaki et al. used rapid thermal processing (RTP) at 450 C° after the deposition of metal pads while my experiments did not include this process.[32] It has been shown that RTP can improve contact resistance due to possible alloying at the interface between metal and semiconductor. [39]Another possible reason for our higher values is the possible extra enhancement of dopant activation at 950 C°. Due to the limited number of samples I had and the need to cover a fair range of temperatures (900 ~ 1100 C°), I was not able to cover any data point in between 900 ~ 1100 C° where the peak of dopant activation might occur. Despite not reproducing as low values of ρ_c and R_c as obtained by Sasaki et al., our values are already good enough for fabricating devices with decent expected performances so the optimized ion-implantation conditions are later used to fabricate MESFETs and MOSFETs on (010)-face epitaxial films.

Since Sasaki et al. reported contact resistance data only on the (010) face, I also did systematic study of the relationship between contact quality and activation temperature for the (-201) face. Same dose of Si ($5*10^{19}$ cm^{-3} box profile) is used from the experiment for (010) face and activation temperature from 800 ~ 1000 C° (in steps of 50 C°) is used to anneal five samples for 30 minutes. The best contact quality is obtained at 900 C° and the results are plotted in Fig. 2.4 (a) and (b). R_c and ρ_c are extracted to be 0.75 Ω-mm and 4.3 $*10^{-5}$ Ω-cm^2, which are very close to those for (010) face, suggesting good feasibility of the same ion-implantation process for (-201). The linearity of I-V characteristic is perfect and sheet resistance is 130 Ω/□, slightly larger than 74 Ω/□ for (010) and 96 Ω/□ for (010) obtained by Sasaki et al.[4] The depth of Si box profiles in our experiments are the same as that in Sasaki el al.'s, both

150 nm.[32] My sheet resistance 74 Ω/☐ is slightly lower than that 96 Ω/☐ from Sasaki et al.[32] possibly due to minor current leakage into the UID substrate because the UID substrates are of n-type (Nd~1*10^{17} cm^{-3}). In my calculation, I have ignored this effect of leakage because the doping of the UID substrate is ~500 times lower than the implanted layer. The resulting good linear scaling between R_{tot} and spacing justifies this assumption. My sheet resistance 130 Ω/☐ for the (-201) face is larger than that 74 Ω/☐ for the (010) face possibly because of the lower activation temperature (900 C° vs 1000 C°) and therefore lower activation efficiency. At 1000 C°, the (-201) face did not reproduce the good linearity of I-V as for (010) face and the ρ_c and R_c are not as good as those at 900 C°. One possible reason for this seemingly inconsistency is that open channels exits in the (-201) direction so at higher temperature, dopant diffusion through these channels into the underling substrate occurs faster than at lower temperatures and as a result, the dopant concentration after activation at the metal-semiconductor interface could be lower for the sample annealed at 1000 C° than that at 9000 C°, resulting in inferior contact quality. Second-ion-mass-spectroscopy (SIMS) can be used to test this proposition but it is not done in this work.

Nonetheless, my experiment produced only ~3 times larger contact resistance compared to the lowest value in literature even without RTP for the (010) face and the R_c and ρ_c obtained for (-201) face using similar Si-ion-implantation process are the first reported values and comparable to those obtained for (010) face.[32] Therefore, this development of Si-ion-implanted Ohmic contact has enabled device fabrication with decent expected performances on both faces.

2.2 MBE regrown contact

Although ion-implantation produced good Ohmic contact quality, it is an expensive, damage-prone process and the high temperature needed to activate the dopants imposes extra challenges for process integration. Therefore, other methods to achieve Ohmic contacts are worth seeking.

MBE regrown contacts have been widely adopted in GaN HEMTs technology because of the high quality of grown films and high dopability in MBE regrown GaN up to ~$1*10^{20}$ cm^{-3}.[40] The Ohmic contacts between the metal and semiconductor can be tremendously enhanced due to tunneling through the barrier. Because reliable and high quality Ohmic contact technology has not been widely realized for Ga_2O_3, it is attractive to explore the possibility of regrown contacts on this material.[32] Ideally, regrown Ga_2O_3 contact layer on Ga_2O_3 substrate by homoepitaxial is the easiest way to obtain high quality film. However, due to the limitation of growing Ga_2O_3 in our MBE chamber, we explore regrowing GaN as contact layer on Ga_2O_3. The motivation behind this are that GaN and Ga_2O_3 have a negligible conduction band offset of ~ 0.1 eV and that imperfect film quality caused by lattice mismatch does not matter as much for contacts as for active region. [42]

A schematic cross-section of the regrown contact is shown in Fig. 2.5. The current goes though the metal/regrown interface, the regrown layer, the regrown/semiconductor interface and then into the Ga_2O_3 . Therefore, the total contact

resistance consists of the contact resistance of each interface and the resistance of the regrown layer. To characterize each of the three components, I fabricate two kinds of devices. For the first sample (Sample 1), an (010) MBE epitaxial film of Sn-doped n-type Ga_2O_3 on semi-insulating (SI) substrate is used and TLM patterns of contact on Ga_2O_3 epilayer is formed by MBE growing n+GaN on a SiO_2 regrowth mask followed by metallization (Fig. 2.6 (a)). For the second sample (Sample 2), the n+GaN layer is blanket-grown on (010) Ga_2O_3 bulk substrate and CTLM patterns of metal contacts are fabricated on the n+GaN (Fig. 2.6 (b)). The detailed step-by-step fabrication process for Sample 1 is illustrated in Fig. 2.7. MBE growth conditions are as follows: 750 C° substrate temperature, 1.89 sccm N_2 flow rate, 200 W RF power for N_2, $1.9*10^{-5}$ Torr chamber pressure, 910 C° Ga cell temperature and 1300 C° Si cell temperature (these results in ~$1*10^{20}$ cm^{-3} doping concentration).

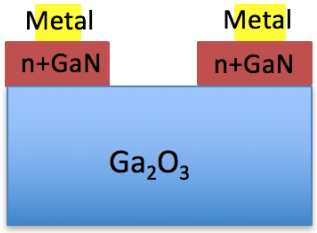

Figure 2.5 Cross-section of and current path through regrown contact.

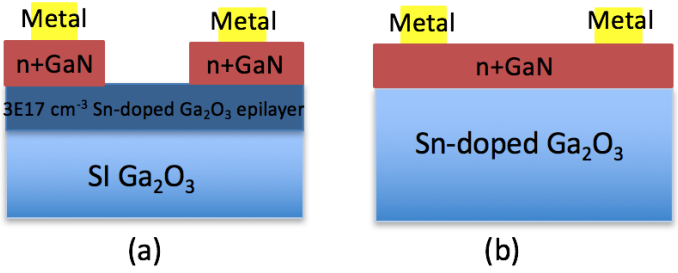

Figure 2.6 (a) Test structure 1 for total R_c; (b) Test structure 2 for metal/regrown R_c.

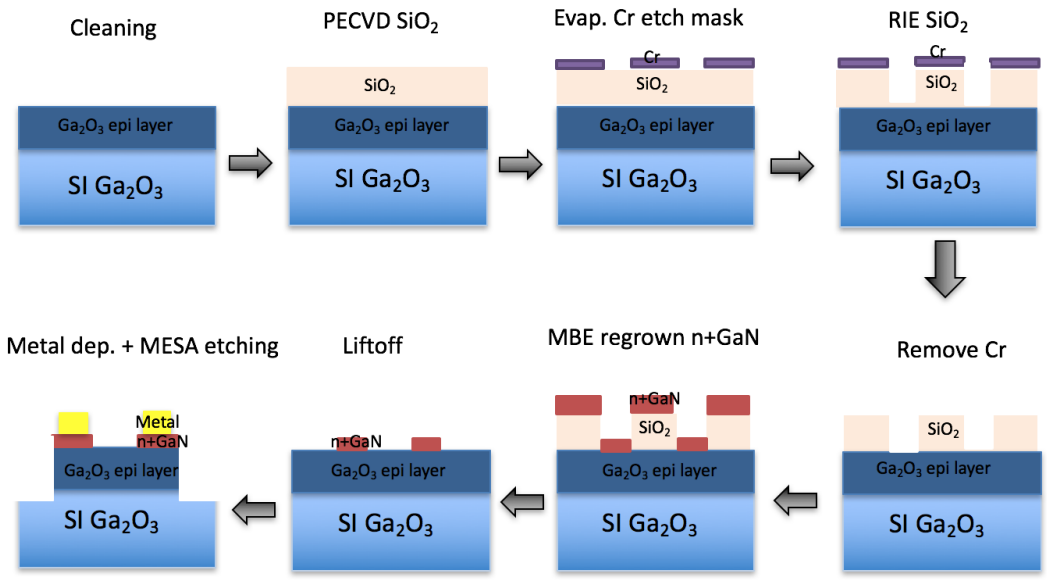

Figure 2.7 Process flow of TLM fabrication for Test Structure 1.

The current level between adjacent contacts of TLM for Sample 1 is very low (~0.3nA/mm at 10V), which is much lower than expected current level from the sheet resistance of the Ga_2O_3 epilayer and decently good contact resistance. This suggests large total contact resistance (R_{tot}), which consists of R_{mr}, R_r and R_{rs}, each representing the metal/regrown contact resistance, the resistance of regrown layer and the regrown/semiconductor contact resistance, respectively. It is hard to tell which component dominates the resistance from just Sample 1 so I-V measurement is also done between the inner and outer contacts of the CTLM test structures on Sample 2. Figure 2.8 (a) shows that the current level is of the same order of that of shorted probes on one metal (blue line), indicating very low total resistance. This results from both small sheet resistance of the highly doped regrown layer, which is related to R_r in Sample 1, and the small contact resistance between metal and regrown layer, which is

the same as R_{mr} in Sample 1. This rules out R_r and R_{mr} from dominating the total contact resistance in Sample 1 and therefore the large R_{tot} in Sample 1 should come

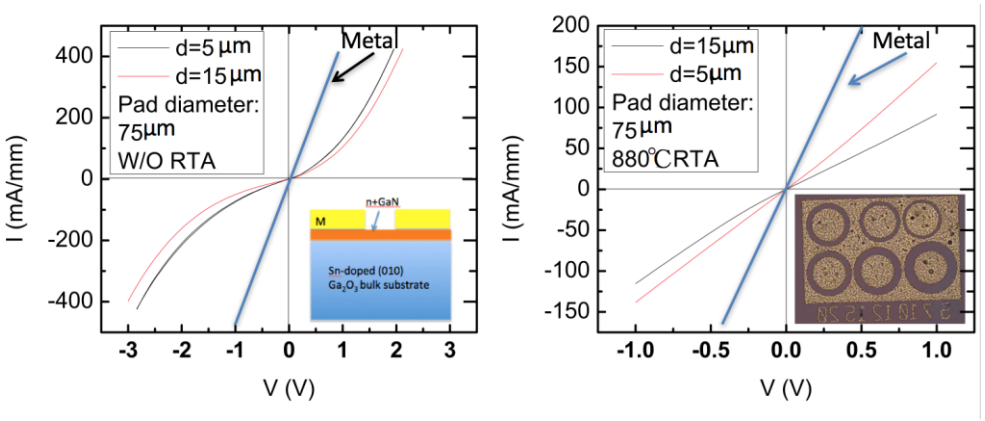

Figure 2.8 (a) I-V of Test Structure 2 without RTP (Inset: cross-section); (b) I-V of Test Structure 2 with RTP (Inset: CTLM; blue line: typical I-V for shorted probes).

from a large R_{rs}. This is inconsistent with the observation of small conduction-band-offset from the XPS data by Wei et al. [42] Theoretically, the regrown n+GaN and Ga_2O_3 should behave as one single material at the conduction band and there should be negligible barrier to current flow from one material to the other. However, the I-V is not consistent with the theoretical prediction possibly due to the following reasons. In Wei et al.'s experiment, the GaN/Ga_2O_3 heterojunction is formed by oxidizing Wurtizte (001) GaN while mine is formed by MBE regrowing GaN on Ga_2O_3.[42] The different methods to grow the same material can cause some variation in material properties like bandgap so the conduction-band-offset in my GaN/Ga_2O_3 junction could be more significant than that in Wei et al.'s. Also, band alignment predicted by XPS does not take into account possible band-shifts caused by space charges at the interface. In actual band alignment between two heterogeneous materials, any defects or polarization at the interface can cumulate carrier charges and therefore alter the

final band alignment. Figure 2.9 and Figure 2.10 show the atomic-force-microscopy (AFM) and X-ray diffraction (XRD) data of the regrown GaN film. The large Root-Mean-Square (RMS) roughness of 3nm suggests bad film quality possibly because of large lattice mismatch (~5%) and therefore a lot of defects such as dangling bonds are expected at the interface.[43] The XRD confirms the (010) orientation of the Ga_2O_3 epilayer and shows that the regrown GaN is of (10-13), a semi-polar face, justifying polarization effect at the interface. The fact that the GaN peak is barely visible with a large Full-width at Half-Maximum (FWHM) again suggests bad film quality.

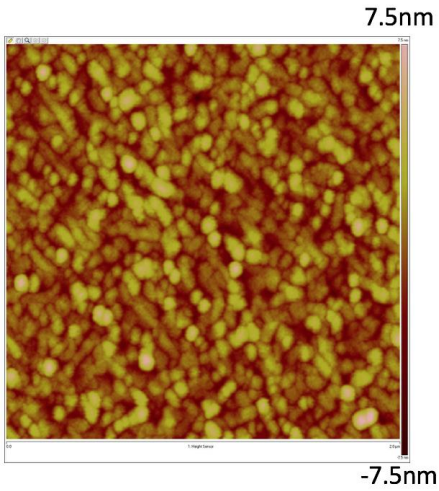

Figure 2.9 AFM of MBE regrown GaN (Scan size: 5 x 5 µm, Scale bar: ±7.5nm, RMS roughness: 3nm).

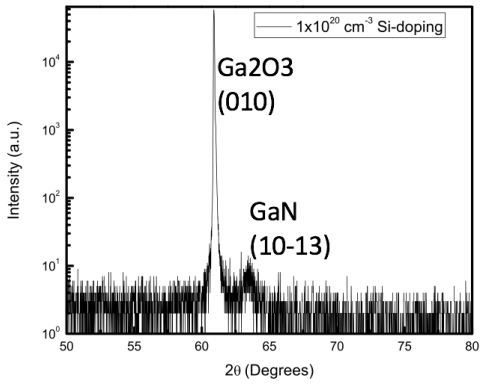

Figure 2.10 XRD of MBE regrown GaN.

Since good Ohmic contact is not achieved with the regrown contact, RTP is used to improve contact quality by possible alloying between GaN and Ga_2O_3. RTP is done at a sequence of temperature (470 C°, 660 C° and 880 C°) in N_2 for 30 seconds at each temperature on Sample 1. After 470 C° and 660 C° RTP, the current level did not improve significantly. After 880 C° RTP, current level improves by ~7 orders of magnitude from before RTP and the I-V is perfectly linear and scaled with spacing (Fig. 2.11 (a)). Figure 2.11 (b) shows the total resistance vs spacing. From similar analysis in Section 2.1, R_c is 35 Ω-mm, ρ_c is $3.85*10^{-4}$ Ω-cm^2 and R_{sh} is $3.2*10^4$ Ω/□ Both R_c and ρ_c are about one order of magnitude higher than those obtained by Si-ion-implantation in Section 2.1. Also, the 880 C° temperature needed to achieve Ohmic contact is not much lower than the activation temperature needed for Si-ion-implanted contact (900 ~ 1000 C°). Therefore, this regrown n+GaN contact is not a preferred method over ion-implantation for Ohmic contacts. Homoepitaxial growth of n+Ga_2O_3 on Ga_2O_3 as contact is expected to have better outcome because the elimination of lattice mismatch and polarization effect and should be studied once growth of highly doped Ga_2O_3 is realized.

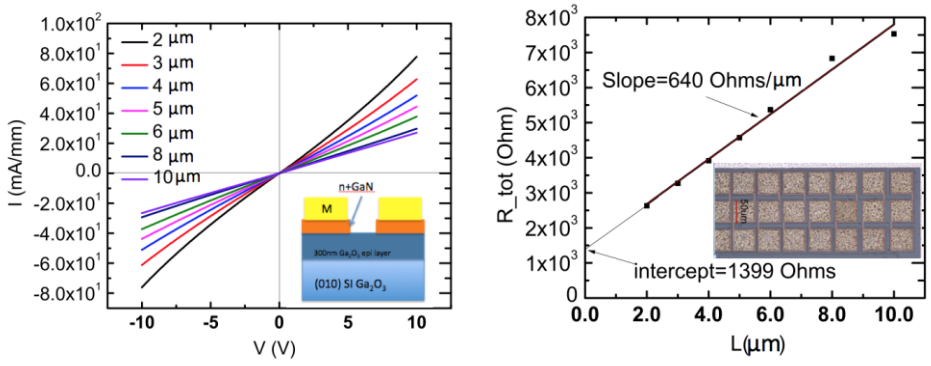

Figure 2.11 (a) I-V of TLM (Inset: Cross-section of test structure); (b) R_{tot} vs d (Inset: Optical image of test structure).

2.3 Benchmark

Figure 2.12 benchmarks our efforts to achieve Ohmic contact in comparison to results from other groups. Our specific contact resistivity is ~1 order of magnitude lower than the best value achieved in literature but it is sufficient for devices with a decent current level.

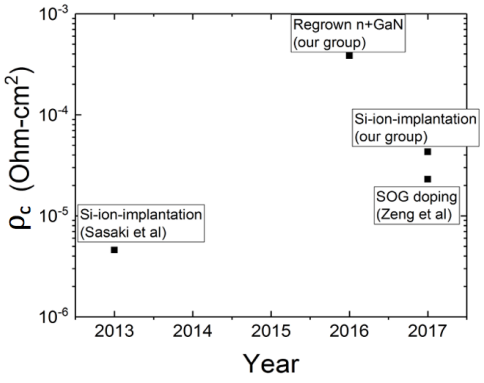

Figure 2.12 Benchmarking of specific contact resistivity.

CHAPTER 3

Dry etching

Dry etching has been extensively used in microelectronic fabrication for its advantages of feature size, tunable etch profile and etch rate over wet etching. In this work, I develop dry etching process using inductively-coupled-plasma reactive-ion etching (ICP-RIE) for Ga_2O_3 aiming at tunable etch rate, vertical sidewalls and minimized damage.

(The entire content of the rest of Chapter 3 is published on JJAP [13]).[2]

In this work, we use a BCl_3/Ar gas mixture to etch Ga_2O_3 because BCl_3 has been shown to etch Ga_2O_3 faster than Cl_2[44] and Ar gives an extra flexibility in tuning relative physical and chemical components. We use ICP to create a high-density plasma that is expected to increase the etch rate and yield smoother surface morphologies than pure RIE.[44] We adjust different parameters in ICP-RIE etching such as ICP power, RIE power, chamber pressure and BCl_3/Ar gas ratio to examine their effects on etch rate, surface morphology and etch profile. Etch rates exceeding ~160 nm/min with nearly-vertical sidewalls and smooth etched surfaces are obtained under the optimal etching conditions.

Experimental details are as follows: 2-in. unintentionally doped (UID; electron concentration ~10^{17} cm^{-3}) Ga_2O_3 wafers of (-201) surface orientation from Tamura Inc. were diced into 5x5mm^2 pieces and cleaned in acetone and isopropanol (IPA) and

[2]

blown dried with N_2. The samples were patterned with AZ S1813 photoresist (PR) using contact photolithography and a mask of various sizes of rectangular strips. The samples were then etched in a Plasma-Therm 770 ICP-RIE system that applies an RF power (ICP power) to a coil to inductively create a high-density plasma and a separate RF power (RIE power) on the chuck to direct the reactive ions to the substrate. To study the effect of each parameter (ICP power, RIE power, chamber pressure and gas ratio), one parameter is varied within a reasonable range while other parameters are kept fixed. The etch rate was measured using a Tencor P-10 surface profilometer. Scanning electron microscopy (SEM) images were then taken at a 79° tilt angle to examine etch profiles and atomic force microscopy (AFM) was used to measure the surface roughness.

Dry etching consists of both physical and chemical etch components. The physical component is from ions bombarding the sample surface. Pure physical etching is anisotropic and can cause severe surface damage and rough surface because of sputtering.[45] Free radicals and ions form highly reactive species that can react with atoms on the sample surface, giving rise to a chemical component of etching. These chemical reactions take place preferably at active sites where there are defects.[45] Pure chemical etching can therefore roughen the surface because of favored reactions and etch byproducts.[45]A synergic mechanism between physical and chemical components usually results in a higher etch rate than each component working individually, because the chemical reaction can help break bonds while physical bombardment can create surface defects and remove etch byproducts to enhance the chemical reaction.[45]Synergic etch has also been shown to result in smooth surface

morphologies because the physical component can help remove etch product and level out protruded features formed by non-uniform chemical reaction.[46] Therefore, if enhanced etch rate and reduced root-mean-square (RMS) roughness are simultaneously achieved, it is an indication of a synergic etch mechanism. In the BCl_3/Ar mixture used in this study, the physical component of etching is from Ar^+ and BCl_3 derived ions bombarding the substrate surface, while Cl free radicals and other highly reactive species from BCl_3 react with atoms on the Ga_2O_3 surface to provide the chemical component of the etching process.

In the first set of experiments, RIE and ICP powers were varied while keeping the BCl_3/Ar gas flows at 35/5 sccm and chamber pressure during etch at 5 mTorr (Fig. 3.1). As shown in Fig. 3.1(a), at high ICP powers (900 W), the etch rate increases significantly with increasing RIE power, indicating that the physical component plays an important role because enhanced ion bombardment can help to remove etch products and simultaneously create surface defects to promote chemical reaction. However, at lower ICP power (350 W), the etch rate stays almost constant with increasing RIE power. This is possibly because at low ICP powers, not many Cl radicals are generated in the plasma and the chemical component is therefore weak. Therefore, an enhanced physical component does not go hand-in-hand with an as-strong chemical one. Moreover, as ICP power increases, the degree to which the etch rate increases with RIE power also increases. At 550 W ICP power, the etch rate increases from 72.6 to 93.5 nm/min (~28% increase) whereas the etch rate increases from 94 to 165 nm/min at 900 W ICP power (~75% increase). For the RIE power of 60 W, the Ga_2O_3 etch rate increases almost linearly with increasing ICP power as

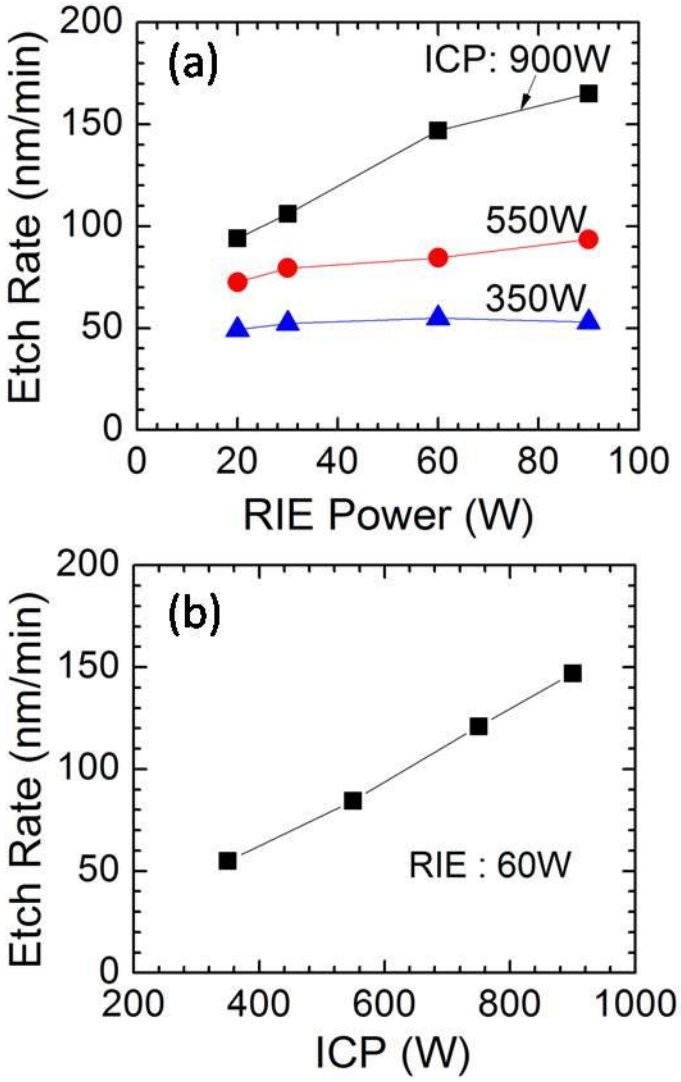

Figure 3.1 (a) Etch rate of UID (-201) β-Ga2O3 vs RIE power at various ICP powers. (b) Etch rate vs ICP power at 60 W RIE power. All etches have been performed at 5 mTorr chamber pressure and BCl3/Ar flowrates of 35/5 sccm.

shown in Fig. 3.1(b). This happens because increasing ICP power will generate more reactive species and positive ions in the plasma, which will enhance both chemical and physical components. By using ICP-RIE etching at high ICP powers, we have obtained ~4x enhancement in the etching rates compared to earlier dry etching studies performed on β-Ga_2O_3.[44,46,47)]

After studying the effect of ICP and RIE powers, I studied the effect of the BCl_3/Ar gas ratio on Ga_2O_3 etch rate. Experiments at following BCl_3/Ar gas flow rates were carried out: 40/0, 35/5, 25/15, 20/20, 15/20 sccm, keeping the total gas flow rate at 40 sccm. ICP and RIE powers of 900 W and 30 W were used for these studies while keeping the chamber pressure at 5 mTorr. The measured etch rates for different gas flow rates are shown in Fig. 3.2. We find that adding Ar to BCl_3 does not change the etch rate significantly till a BCl_3/Ar flow rate of 25/15 sccm. Further increase in the Ar

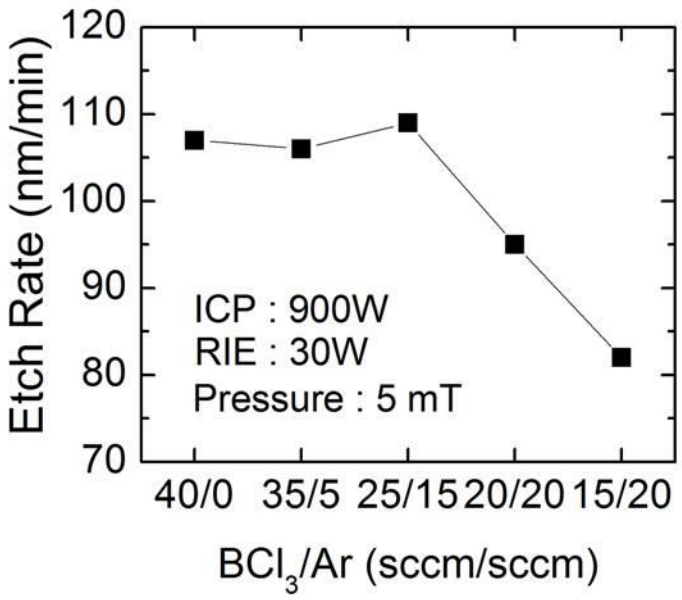

Figure 3.2 Etch rate of UID (-201) β-Ga2O3 vs BCl3=Ar flow rate at 5 mTorr chamber pressure, 30W RIE and 900 W ICP powers.

flow rate decreases the etch rate. Ar is expected to promote physical etching because Ar+ ions can help remove etch products and creating active sites for chemical etching. If BCl_3 only provides chemical component by producing the reactive Cl radical, adding Ar to pure BCl_3 would enhance etch rate because of synergic mechanism. A

previous study found that BCl_3 produces heavy BCl^{+2} and BCl^{+3} ions that do physical etching as well.[48]Therefore, BCl_3 by itself can provide both chemical and physical etch components in the plasma to promote the synergic mechanism. As more Ar is added, the etch rate eventually drops because of the lack of Cl radical. The etch rate in pure Ar was not obtained because the plasma could not be lit at same ICP/RIE powers and pressure. However, following the trend in Fig. 3.2, further reduction in the etch rate is expected for pure Ar. Liang et al. have performed a similar study of Ga_2O_3 etching with a SF_6/Ar mixture that shows a trend similar to Fig. 3.2 and negligible etch rate with pure Ar.[46]

In the last set of experiments, we studied the effect of chamber pressure on (-201) β-Ga_2O_3 etch rate while the ICP/RIE powers are kept at 900 W/90 W and BCl_3/Ar flow rate at 35/5 sccm. As shown in Fig. 3.3, the etch rate decreases when the chamber pressure increases from 5 to 12 mTorr. At higher pressures, more collisions occur between particles leading to a reduced mean-free path and recombination of free radicals. This enhanced recombination leads to less chemically reactive species and reduced chemical component of etching.[45] Further, the reduced DC bias across the sheath at higher pressures reduces ion bombardment energies and therefore the physical component. Reduction in both physical and chemical components leads to the decrease in etch rate at higher chamber pressures.

The morphology of the sample surface before and after etching is studied using AFM. The RMS roughness is compared across different etching conditions mentioned in previous paragraphs. The effect of increasing RIE power on the RMS roughness is shown in Fig. 3.4(a). With increasing RIE power, the etched surface maintains roughly

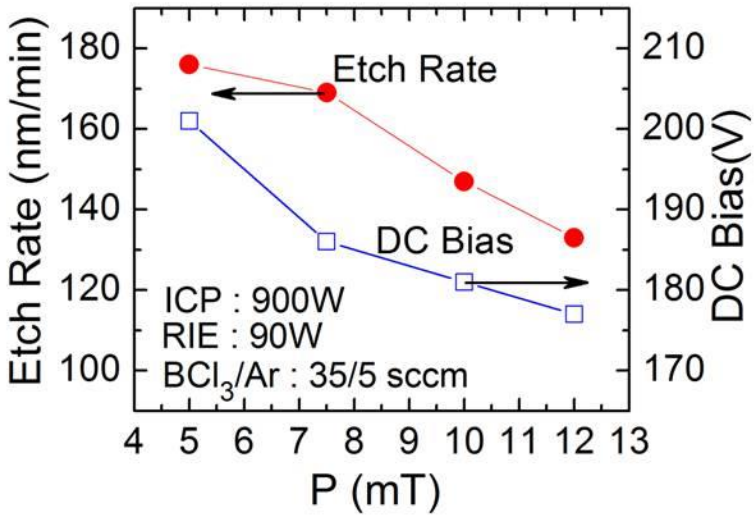

Figure 3.3 Etch rate (left-axis) of UID (-201) β-Ga2O3 and DC bias voltage (right-axis) vs chamber pressure at 900 W ICP, 90 W RIE, and 35/5 sccm BCl3/Ar flow rate.

the same roughness as the unetched surface, suggesting that the etching has caused minimal surface damage. The RMS roughness even decreases slightly as the RIE power increases beyond 60 W, indicating that a balance is reached between the physical and chemical etching components. This reduced RMS at higher RIE is consistent with the enhanced etch rate at higher RIE, both being evidences for synergic mechanism.

Figure 3.4(b) shows the influence of the BCl_3/Ar flow rate on sample roughness. When BCl_3 flow rate is greater than or equal to Ar flow rate, the RMS roughness does not change much from the unetched sample (RMS: 0.256 nm), indicating synergic etching. However, for BCl_3/Ar flow rate of 15/25 sccm, RMS roughness increases drastically to 54.8 nm. This abrupt increase in roughness is probably because there are not enough Cl radicals in this condition to do chemical etching and the physical and chemical etch components go out of balance. Pure BCl_3

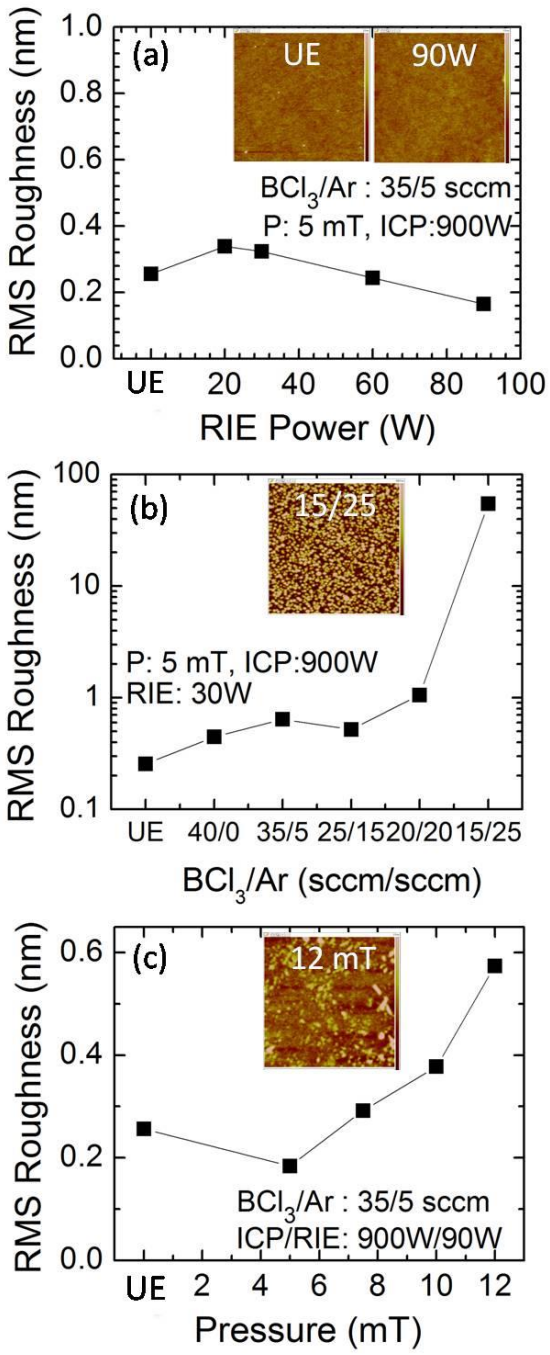

Figure 3.4 (a) RMS roughness of unetched (UE) UID (-201) β-Ga2O3 sample and samples etched under different RIE powers (inset: AFM image of UE and 90 W RIE sample, height scale bar: ±2 nm, scan size: 5 × 5 μm^2), (b) RMS roughness for UE sample and samples etched with different BCl3/Ar gas flows (inset: AFM image of BCl3/Ar 15/25 sccm sample, height scale bar: ±100 nm, scan size: 5 × 5 μm^2), (c) RMS roughness for UE sample and samples etched at different chamber pressures (inset: AFM image of 12 mTorr sample, height scale bar: ±2 nm, scan size: 5 × 5 μm^2).

results in an RMS as good as the mixture of BCl_3 and Ar, confirming that BCl_3 provides BCl^{+2} and BCl^{+3} ions that also perform physical etching. This is consistent with the etch rate data shown in Fig. 2.2 that shows that pure BCl_3 etches as fast as BCl_3/Ar mixture.

The RMS roughness increases only slightly with increase of chamber pressure as shown in Fig. 3.4(c), suggesting that synergic etch mechanism is maintained in the 5 -12 mTorr chamber pressure range. From these studies, we identify a large window of ICP-RIE etching conditions under which very smooth surface morphologies with sub 1 nm RMS roughness for 5x5μm^2 scans can be obtained. This finding will be crucial for device fabrication, if can be combined with sharp etched sidewalls.

SEM images were taken at a tilt angle of 79° to examine the etch profile and sidewalls of the (-201) β-Ga_2O_3 under all etch conditions. Smooth and nearly vertical sidewalls were obtained for the samples etched under the synergic mechanism. Figure 3.5 shows the SEM image of the sample etched at 350 W/60 W ICP/RIE, 5 mTorr chamber pressure and 35/5 sccm BCl_3/Ar flow rate. Because physical etching is anisotropic and chemical etching is isotropic,[45)] the synergic etching occurs only on the surface of substrate and chemical etching on the sidewalls. Because synergic etching is much faster than chemical etching acting alone,[45)] etching in the vertical direction dominates and creates vertical sidewalls.

In this work, we systematically study the effects of various etch parameters on etch rate, surface morphology and etch profile of β-Ga2O3. RIE, ICP powers, chamber pressure and gas mixture ratio are shown to have prominent impacts on etch rate. A synergic etching mechanism between chemical and physical components is confirmed.

This mechanism can provide higher etch rate and smoother surface than either chemical or physical component acting individually. The etch parameters have been shown to be tunable to balance physical and chemical components to achieve smooth surface and nearly vertical profile. This is important for the processing of vertical power devices with high performances.

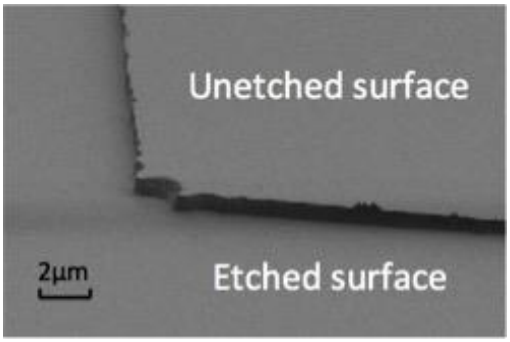

Figure 3.5 SEM image of etched Ga2O3 showing vertical sidewalls and smooth etched surface (ICP/RIE 900W/60W, Chamber pressure 5mT, BCl3/Ar 35/5 sccm).

CHAPTER 4

Device Applications

In this chapter, the Ohmic contact and the dry etching processes optimized in the proceeding chapters are used to fabricate field-effect transistors. In Section 4.1, lateral devices such as MOSFETs are studied integrating the ion-implantation process for Ohmic contacts. Current modulation of ~10^6 is achieved. In Section 4.2, vertical FinFETs are studied integrating the dry etch process to make fin-structures with vertical sidewalls. Minor current modulation is observed and further improvement in device structure design and integration of ebeam lithography (EBL) to make fins with reduced dimensions can further enhance current modulation.

Section 4.1 MOSFETs

MBE-grown Epilayer with 100nm thickness and ~$2x10^{17}$ cm^{-3} n-type doping (Si as dopants) on Fe-doped semi-insulating substrate is used to fabricate MOSFETs. The substrate cross-section and the process flow are illustrated in Fig. 4.1. First, Ohmic contact is formed by applying Si-ion-implantation in the source and drain region. Instead of a box-profile, a single does resulting in peak n-type doing of $5x10^{19}$ cm^{-3} is used followed by 30 minutes of 1000 °C activation in an annealing furnace. The peak is made to occur at the Ga2O3 surface by ion-implanting with a 40 nm SiO_2 cap deposited by PECVD. Following removal of the SiO_2 by hydrofluoric acid (49% HF), metal contacts are made to the n+ regions by ebeam evaporating Ti/Au (20nm/100nm) metal stacks. No post-deposition annealing is done. Silicon alignment marks was fabricated even before ion-implantation to assist aligning the Ti/Au metal

stacks to the ion-implanted regions. Mesa isolation is done using ICP-RIE with a BCl_3/Ar gas mixture (see Chapter 3). A depth of 180 nm of mesa is etched to ensure sufficient device isolation. The device is characterized (TLM for contact resistance, 2T I-V measurement for S/D current pre-gate-deposition) before the final step of gate fabrication.

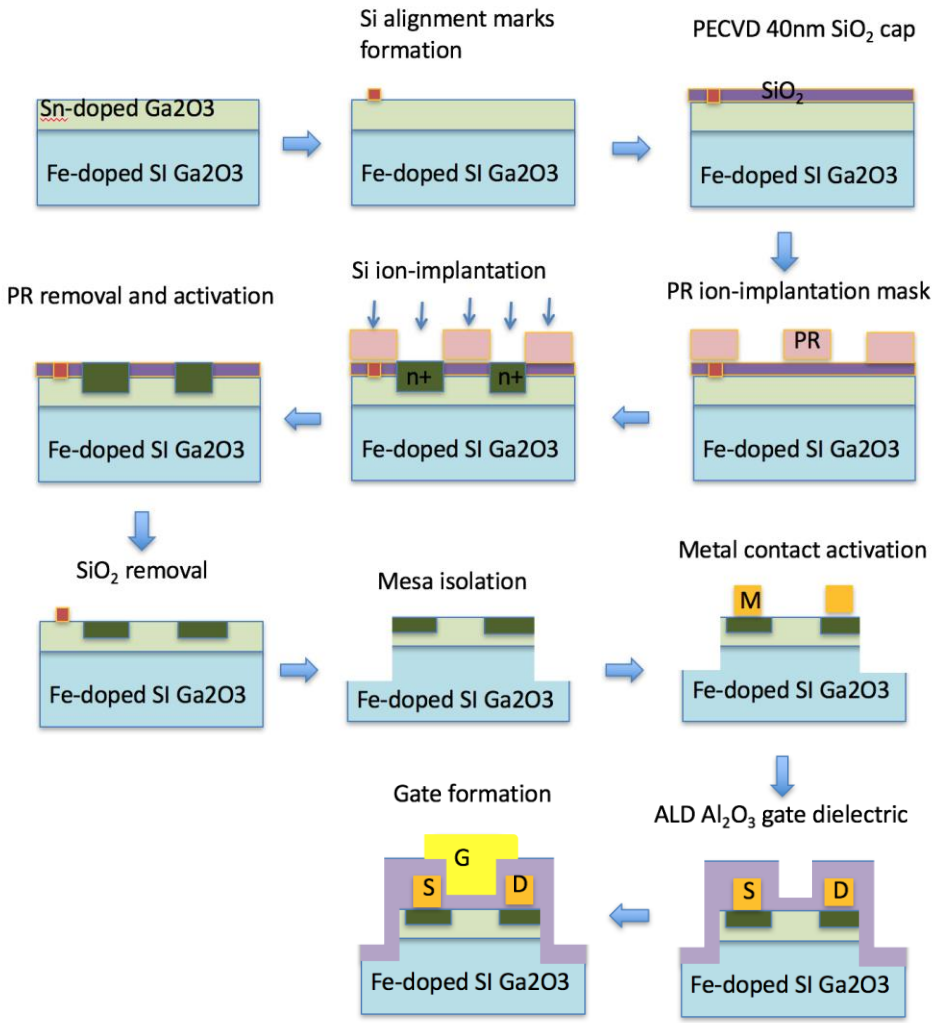

Figure 4.1 Process flow for MOSFETs.

Figure 4.2 (a) and (b) show the I-V curves for TLM on Si-ion-implanted n+Ga2O3 and TLM on un-implanted n-Ga2O3, respectively. The cross-sections for these two kinds of TLM structures are displayed along with the corresponding I-V plots. The current level in the TLM-on-n+Ga2O3 test structure is in the same

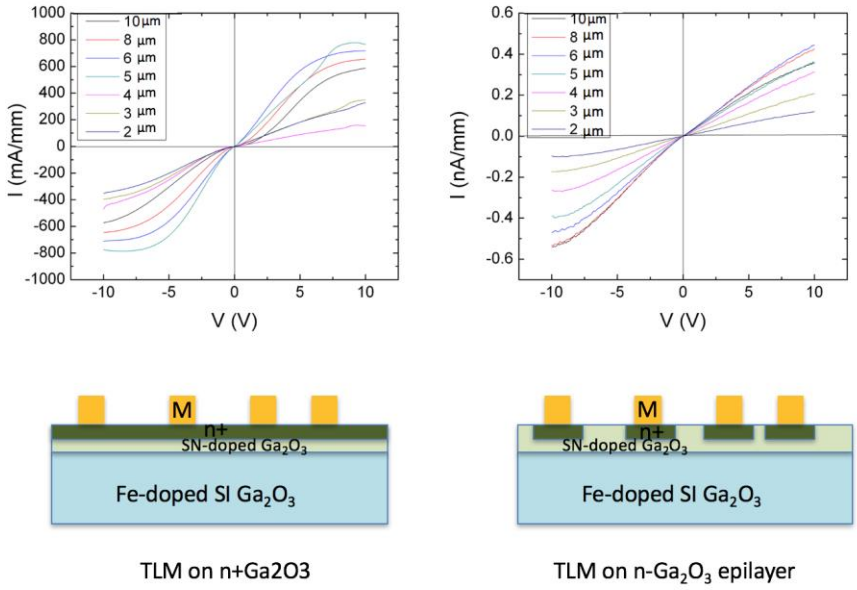

Figure 4.2 TLM test structures and I-V curves for (a) n+Ga_2O_3; (b) n-Ga_2O_3 epilayer.

order of magnitude as those in the CTLM-on- n+Ga2O3 structures in Chapter 2, indicating good Ohmic contact after dopant activation. The linearity of the I-V is not as perfect as those in Chapter 2 possibly due to the single-dose ion-implantation for which minor error in the SiO2 thickness can cause significant shift of the concentration peak from the surface. Therefore, Schottky-like behavior is observed in the I-V. In contrast, the current level in the TLM test structure in Fig 4.2(b) is only ~0.5 nA/mm, ~9 orders of magnitude lower than that in the TLM in Fig 4.2(a). This current level is also ~8 orders of magnitude lower than expected current density calculated from the doping concentration, the thickness and a 100 cm^2/V-s mobility of

the channel. Device channels with similar doping and dimensions reported in the literature have shown ~10s mA/mm current density.[10)] Apparently, the channel has become insulating during the process of ion-implantation and activation. Wong et al studied the anomalous Fe diffusion in Si-ion-implanted Ga2O3 using similar doping and activation time and temperature. [44)] They used 300 nm MBE-grown Ga_2O_3 epilayer on similar Fe-doped SI substrate for their study and the doping of their epilayer and SI substrate are both similar to ours. [44)] After 30 min 950°C activation, their entire 300 nm epilayer was compensated by Fe, which is a deep- level trap.[44)] Since I used similar Si-ion-implantation and activation conditions and my epilayer is only 100 nm thick, the insulating channel can be explained by the Fe-out-diffusion. Also, from SIMS characterization, Wong et al found that the Fe that diffused into the epilayer has the same order of magnitude of doping as the epilayer (~1E17 cm-3).[44)] Therefore, only the n-Ga_2O_3 in my structure is compensated but the n+Ga_2O_3 (~5E19 cm^{-3}) remains high conductive so the current level in the TLM structure on n+Ga_2O_3 (Fig 4.2(a)) remains high.

Because the channel is now insulating, a lateral MESFET cannot be realized on this structure anymore. Therefore, a MOS-gate with the gate area overlapping with the source and drain is fabricated (see Fig 4.1). A 24 nm thick Al2O3 is deposited by atomic-layer deposition (ALD) and then a Ti/Pt/Au (3/50/150 nm) gate metal stack is deposited by ebeam evaporation. The overlapped length is 1 μm. The source and drain metals are probed by scratching the thin Al2O3 with probes gently.

Figure 4.3 shows the transfer behaviors for three measured MOSFETs in both linear and log scales. The devices behave as enhancement-mode (E-mode) in which the channel appears off with very low current at zero gate bias. The channel is turned

on as positive gate bias is ramped up. Most of the measured devices breakdown (gate current spikes to compliance) at 9~10 V V_{gs}. The best device (Dev 2 in Fig 4.3) has a peak channel current of 0.004mA/mm at 9 V V_{gs} and therefore a ~10^6 On/Off ratio. From the transfer curves, the E-Mode devices turn on at around 4.5 V V_{gs}, which suggests the deep traps at the surface have now been filled with electrons and there is a conducting channel forming on the surface.

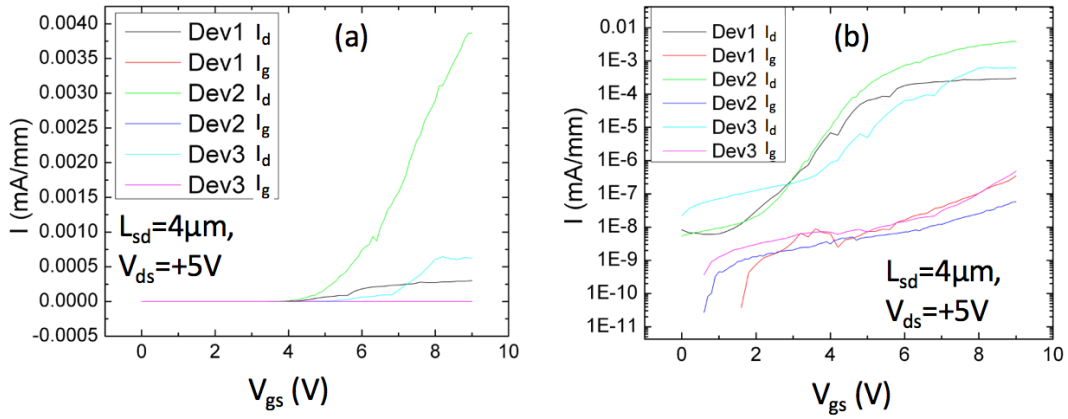

Figure 4.3 Transfer curve for MOSFET in (a) linear scale; (b) log scale.

Figure 4.4 shows the family curve for the MOSFET (the devices in Fig 4.3 breakdown at 9 V so the family curve is taken on a fresh device). The drain current saturates at ~1V Vds. The peak current is ~1.25 x 10^{-4} mA/mm at 6 V Vgs. The current tends to droop after current saturation but heating of the material at this low current level is unlikely to cause such droop. Therefore, the reason for the drooping is unclear. The same device has an off-state breakdown voltage of ~15 V shown in Fig 4.5.

Overall, the device current is about 4 ~ 5 orders of magnitude lower than those published.[10)] This is due to the limited gate bias that can be applied to modulate the channel current due to the quality of gate dielectric and also the applied gate voltage is

first used to fill the traps and then used to turn on the channel at the interface. Improvement in gate modulation can be achieved by optimizing gate dielectric and eliminating traps in the material by using a buffer layer to suppress out-diffusion of Fe from the substrate.[44)]

The off-state breakdown voltage in this device is limited by the direct overlapping between the gate and S/D metal separated by only by the gate dielectric. For E-mode device, the structure can be improved by leaving an access region of n+Ga2O3 to overlap with the gate metal but recessing the S/D metal. For minimizing the conduction loss in the prolonged access region, self-aligned process can be implemented to minimize this loss.

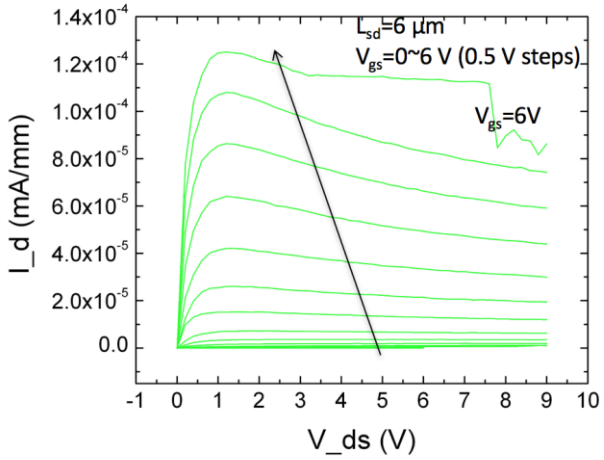

Figure 4.4 Family curve for MOSFETs.

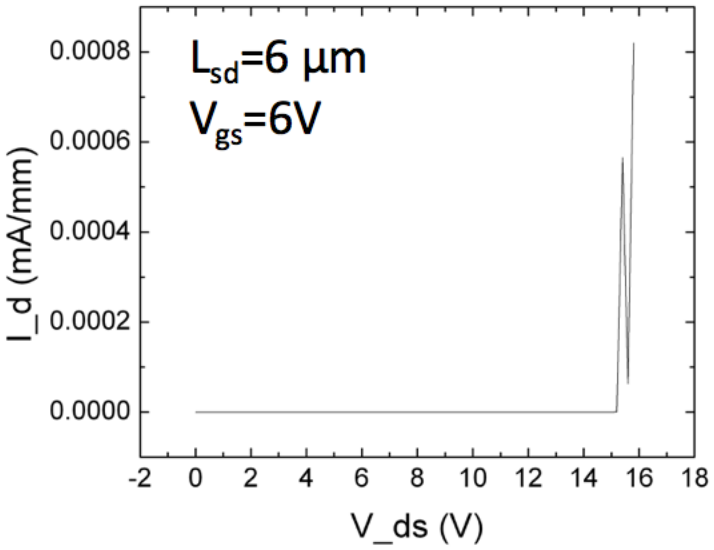

Figure 4.5 Off-state breakdown voltage.

Section 4.2 Vertical FinFETs

Vertical FinFETs are made by dry etching Ga_2O_3 substrates to create standing fin-shaped channels. The dry etch process from Chapter 3 was used to create fins with vertical sidewalls and width from 2 ~ 3 µm. Source metal contact Ti/Pt 20/100 nm was deposited prior to dry etch and subsequently worked as a self-aligned etch mask. About 1 µm depth was etched. For ionic-gating devices, gate pads Ti/Pt 20/100 nm are deposited on SiO_2 insulating layer deposited on the substrate by PECVD and then the electrolyte is spun on the substrate to make ionic gate. A schematic of the device is shown in Fig 4.6.

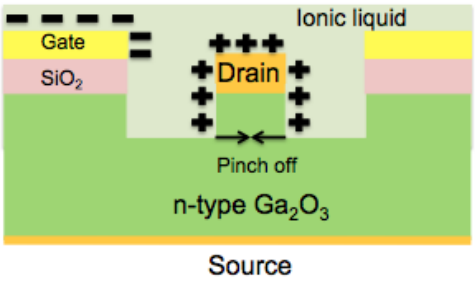

Figure 4.6 Cross-section of ionic-gated FET.

Transfer characteristic is shown in Fig 4.7. Less than 5% of current modulation was observed possibly due to the limited gate voltage that could be applied to the electrolyte (< -1.2V) and large channel width.

Solid-gate FET was made by the same process as in ionic-gated FETs. Then, ~6 nm Al_2O_3 gate dielectric was deposited on the sidewalls by plasma-assisted atomic layer deposition (ALD) and subsequently ~3 nm Pt on Al_2O_3 by thermal ALD as gate metal. The gate metal is then connected to thick metal pads by ebeam evaporating 80 nm Pt on top of the 3 nm Pt gate metal already deposited. Fig 4.8 shows the schematic of the solid-gate FET.

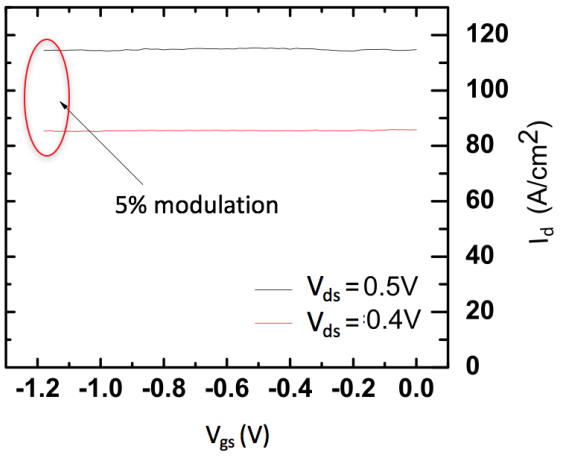

Figure 4.7 Transfer characteristics of ionic-gated FET.

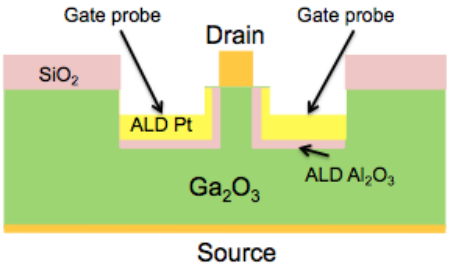

Figure 4.8 Cross-section of solid-gate FET.

Three-terminal measurement is shown in Fig. 4.9. In the negative V_{ds} region, the current decreases with increasing negative gate bias but the gate current (not shown here) is of the same order as the channel current in this region. Therefore, the seemingly current modulation is more likely due to gate injection instead of gate modulation. Also, because the there is no current modulation observed in the positive V_{ds} region, where gate current is orders of magnitude lower than the channel current, current injection in the negative V_{ds} region is further confirmed.

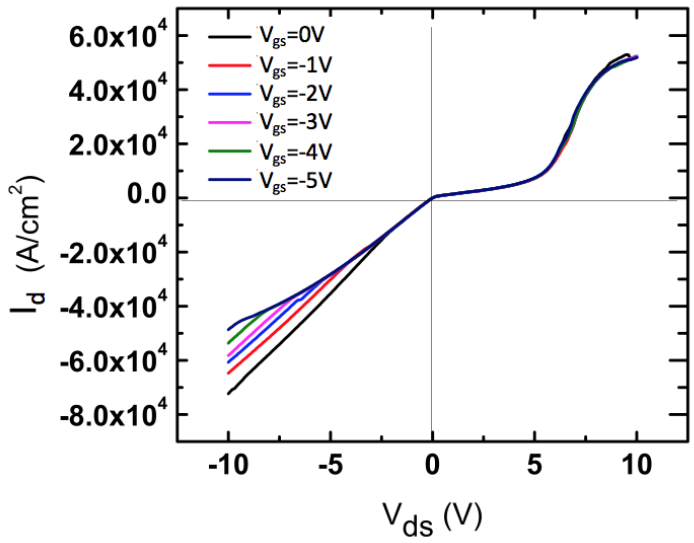

Figure 4.9 Output characteristic of solid-gate FET.

Improvements in the performances of device can be made by shrinking channel width to ~100 nm so it can be pinched off at moderate gate voltage. Use of edge termination at the bottom of fins can further enhance breakdown voltage.

CHAPTER 5

Conclusion

This work has experimentally optimized the Ohmic contact and dry etching processes for electronic device fabrication on β-Ga_2O_3. Si-ion-implantation method achieved <1 Ω-mm contact resistance and specific contact resistivity of the order of 10^{-5} Ω/□ for both (010) and (-201) faced substrates. This process can effectively reduce the conduction loss across the contacts and access regions. This work also identified a wide process window where physical and chemical etching work in a synergic fashion so that controllable etch rate, vertical sidewall and minimized damage can be achieved with well-controlled dry etching. These results have great impacts on fabrication of vertical devices with a free-standing fin as channel, which is popular for vertical high-power devices for other material systems. The performances of MOSFETs are explored implementing the Si-ion-implantation process for Ohmic contact and the devices had ~10^6 On/Off ratio, suggesting clear transistor action. The channel current level is relatively low (~0.001 mA/mm) due to donor compensation by the Fe, a deep-level trap, diffusing out from the substrate following high-temperature activation and a limited gate bias that could be applied due to the limitation of gate dielectric. Further improvement of device performances can be achieved by using a buffer layer to suppress the Fe-out-diffusion and optimizing gate dielectric. Vertical wrap-around gate fin-channel FETs (vFinFETs) are studied using the dry etch process developed in this work and vertical fin-shaped channel with vertical sidewalls is successfully fabricated. Both ionic-liquid and solid wrap-around gate are used to

explore the channel modulation under gate bias. The channel current modulation is only minor (<5% for ionic gate and for solid gate, it is unclear if the modulation seen is due to gate modulation or injection). Reasons for the small modulation are large channel width limited by photolithography and limited gate voltage that can be applied. EBL can be used to create fin width down to 100 nm, which from simulation can be pinched-off under a moderate gate bias. Gate dielectric can be further optimized by eliminating traps and optimizing thickness. Better Ohmic contact can be achieved on the small contact area on the top of the fin (source contact) using Si-ion-implantation. Edge termination at the bottom of the fin can be implemented to smooth out high electric field to boost breakdown voltage. Overall, due to the unique properties of β-Ga_2O_3, and the promise this material is already showing as a conducting channel, β-Ga_2O_3 should be further pursued for its high-power capability for future power electronics.

REFERENCES

1) Mimura, T., et al. "A new field-effect transistor with selectively doped GaAs/n-$Al_xGa_{1-x}As$ heterojunctions." Japanese Journal of Applied Physics 19.5 (1980): L225.

2) Duan, X., et al. "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices." Nature 409.6816 (2001): 66-69.

3) Nakamura, S., et al. "Candela-class high-brightness InGaN/AlGaN double-heterostructure blue-light-emitting diodes." Applied Physics Letters 64.13 (1994): 1687-1689.

4) Chowdhury, S., et al. "Current status and scope of gallium nitride-based vertical transistors for high-power electronics application." Semiconductor Science and Technology 28.7 (2013): 074014.

5) Ohta, H., et al. "Frontier of transparent oxide semiconductors." Solid-State Electronics 47.12 (2003): 2261-2267.

6) Kokubun, Y., et al. "Sol-gel prepared β-Ga_2O_3 thin films for ultraviolet photodetectors." Applied Physics Letters 90.3 (2007): 031912.

7) Hudgins, J. L., et al. "An assessment of wide bandgap semiconductors for power devices." *IEEE Transactions on Power Electronics* 18.3 (2003): 907-914.

8) Marckx, D. A. “Breakthrough in power electronics From SiC.” Subcontract Rep. NREL/SR-500-38515 (2006).

9) Baliga, B. J. "Gallium nitride devices for power electronic applications." Semiconductor Science and Technology 28.7 (2013): 074011.

10) Higashiwaki, M., et al. "Recent progress in Ga_2O_3 power devices." Semiconductor Science and Technology 31.3 (2016): 034001.

11) Galazka, Z., et al. "Czochralski growth and characterization of β-Ga_2O_3 single crystals." Crystal Research and Technology 45.12 (2010): 1229-1236.

12) Galazka, Z., et al. "Melt growth and properties of bulk $BaSnO_3$ single crystals." Journal of Physics: Condensed Matter 29.7 (2016): 075701.

13) Aida, H., et al. "Growth of β-Ga_2O_3 single crystals by the edge-defined, film fed growth method." Japanese Journal of Applied Physics 47.11R (2008): 8506.

14) Ueda, N., et al. "Synthesis and control of conductivity of ultraviolet transmitting β-Ga_2O_3 single crystals." Applied Physics Letters 70.26 (1997): 3561-3563.

15) Víllora, E. G., et al. "Large-size β-Ga_2O_3 single crystals and wafers." Journal of Crystal Growth 270.3 (2004): 420-426.

16) Higashiwaki, M., et al. "Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3 (010) substrates." Applied Physics Letters 100.1 (2012): 013504.

17) Sasaki, K., et al. "Ga_2O_3 Schottky Barrier Diodes Fabricated by Using Single-Crystal Ga_2O_3 (010) Substrates." IEEE Electron Device Letters 34.4 (2013): 493-495.

18) Song, B., et al. "Vertical Ga_2O_3 Schottky barrier diodes on single-crystal β-Ga_2O_3 (−201) substrates." Device Research Conference (DRC), 2016 74th Annual. IEEE, 2016.

19) Konishi, K., et al. "Ga_2O_3 field-plated Schottky barrier diodes with a breakdown voltage of over 1 kV." Device Research Conference (DRC), 2016 74th Annual. IEEE, 2016.

20) Varley, J. B., et al. "Role of self-trapping in luminescence and p-type conductivity of wide-band-gap oxides." Physical Review B 85.8 (2012): 081109.

21) Chowdhury, S., et al. "Current status and scope of gallium nitride-based vertical transistors for high-power electronics application." Semiconductor Science and Technology 28.7 (2013): 074014.

22) Sun, M., et al. "Vertical GaN power FET on bulk GaN substrate." Device Research Conference (DRC), 2016 74th Annual. IEEE, 2016.

23) Zhang, L., et al. "Inductively-coupled-plasma reactive ion etching of single-crystal β-Ga_2O_3." Japanese Journal of Applied Physics 56.3 (2017): 304.

24) Wong, M. H., et al. "Field-plated Ga_2O_3 MOSFETs with a breakdown voltage of over 750 V." IEEE Electron Device Letters 37.2 (2016): 212-215.

25) Chabak, K. D., et al. "Enhancement-mode Ga_2O_3 wrap-gate fin field-effect transistors on native (100) β-Ga_2O_3 substrate with high breakdown voltage." Applied Physics Letters 109.21 (2016): 213501.

26) Hwang, W. S., et al. "High-voltage field effect transistors with wide-bandgap β-Ga_2O_3 nanomembranes." Applied Physics Letters 104.20 (2014): 203111.

27) Zhou, Hong, et al. "High-performance depletion/enhancement-mode β-Ga_2O_3 on insulator (GOOI) field-effect transistors with record drain currents of 600/450 mA/mm." IEEE Electron Device Letters 38.1 (2017): 103-106.

28) Zhou, H., et al. "β-Ga_2O_3 on insulator field-effect transistors with drain currents exceeding 1.5 A/mm and their self-heating effect." arXiv preprint arXiv:1703.06197 (2017).

29) Green, A. J., et al. "3.8-MV/cm Breakdown Strength of MOVPE-Grown Sn-Doped β-Ga_2O_3 MOSFETs." IEEE Electron Device Letters 37.7 (2016): 902-905.

30) Oshima, T., et al. "Formation of indium–tin oxide ohmic contacts for β-Ga_2O_3." Japanese Journal of Applied Physics 55.12 (2016): 1202B7.

31) Zeng, K., et al. "Ga 2 O 3 MOSFETs Using Spin-On-Glass Source/Drain Doping Technology." IEEE Electron Device Letters 38.4 (2017): 513-516.

32) Sasaki, K., et al. "Si-ion implantation doping in β-Ga2O3 and its application to fabrication of low-resistance ohmic contacts." Applied Physics Express 6.8 (2013): 086502.

33) Liang, H., et al. "A preliminary study of SF 6 based inductively coupled plasma etching techniques for beta gallium trioxide thin film." Materials Science in Semiconductor Processing 39 (2015): 582-586.

34) Zhou, Y., et al. "Formation, etching and electrical characterization of a thermally grown gallium oxide on the Ga-face of a bulk GaN substrate." Solid-State Electronics 52.5 (2008): 756-764.

35) Hogan, J. E., et al. "Chlorine-based dry etching of β-Ga_2O_3." Semiconductor Science and Technology 31.6 (2016): 065006.

36) Yang, J., et al. "Inductively coupled plasma etch damage in (-201) Ga_2O_3 Schottky diodes." Applied Physics Letters 110.14 (2017): 142101.

37) Ohira, S. and Arai, N. "Wet chemical etching behavior of β-Ga_2O_3 single crystal." physica status solidi (c) 5.9 (2008): 3116-3118.

38) Oshima, T., et al. "Wet etching of β-Ga_2O_3 substrates." Japanese Journal of Applied Physics 48.4R (2009): 040208.

39) Foresi, J. S., and Moustakas, T. D. "Metal contacts to gallium nitride." Applied Physics Letters 62.22 (1993): 2859-2861.

40) Yue, Y., et al. "InAlN/AlN/GaN HEMTs with regrown Ohmic contacts and f_T of 370 GHz." IEEE Electron Device Letters 33.7 (2012): 988-990.

41) Higashiwaki, M., et al. "Recent progress in Ga2O3 power devices." Semiconductor Science and Technology 31.3 (2016): 034001.

42) Wei, W., et al. "Valence band offset of β-Ga_2O_3/wurtzite GaN heterostructure measured by X-ray photoelectron spectroscopy." Nanoscale Research Letters 7.1 (2012): 562.

43) Víllora, E. G., et al. "Epitaxial relationship between wurtzite GaN and β-Ga_2O_3." Applied Physics Letters 90.23 (2007): 234102.

44) Hogan, J. E., et al. "Chlorine-based dry etching of β-Ga_2O_3." Semiconductor Science and Technology 31.6 (2016): 065006.

45) Plummer, J.D., Deal, M., and Griffin, P.B. *Silicon VLSI Technology*: *Fundamentals, Practice, and Modeling* (Prentice Hall, Upper Saddle River, NJ, 2000) 1st ed., Chap. 10.

46) Liang, H., et al. "A preliminary study of SF 6 based inductively coupled plasma etching techniques for beta gallium trioxide thin film." Materials Science in Semiconductor Processing 39 (2015): 582-586.

47) Zhou, Y., et al. "Formation, etching and electrical characterization of a thermally grown gallium oxide on the Ga-face of a bulk GaN substrate." Solid-State Electronics 52.5 (2008): 756-764.

48) Rawal, D. S., et al. "BCl_3/Cl_2-Based Inductively Coupled Plasma Etching of GaN/AlGaN Using Photoresist Mask." IEEE Transactions on Plasma Science 40.9 (2012):2211-2220.